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Study on Ultra Shallow Junction n-MOS with 350°C Microwave Annealing for Activation of Phosphorus Dopants in Germanium

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Abstract: In this study, low-energy microwave annealing is used to fabricate ultra-shallow junctions for less than 20 nm IC node applications in a potential material: Germanium (Ge). Germanium is a new promising material and might replace silicon in the future. A novel microwave annealing technique with two steps for the solid phase epitaxial recrystallization (SPER) and phosphorus dopants activation was applied to Germanium. The purpose of the first step, microwave annealing of 1.2 kW for 75 s, is to re-grow the amorphous layer and repair the destroyed crystal lattices caused by ion implantation. In the second-step of annealing, low-energy microwave, 0.9 kW (≈350°C) for 300 s, is used to activate the phosphorus dopants effectively without diffusion and de-activation. The target dopant activation concentration level will achieve 10^{20} cm^{-3}. The sheet resistance will decrease to 78 ohm/sq. The low resistance after activating is reflected to the performance of the n-MOS device fabricated by the Ge substrate. The S. S. factor is 900 mV/dec, and the $I_{on/off}$ ratio rise to 2.6×10^{1}. This has demonstrated that the two-step MWA has excellent control, significantly regarding leakage current.

Keywords: Activation, Germanium, Implant, Microwave Annealing, Solid Phase Epitaxial Recrystallization (SPER)

1. Introduction

As semiconductor devices scale down, the gate length decreases. For future complementary metal-oxide semiconductor (CMOS) devices, scaling limiting becomes the main challenge, such as the formation of annealed ultra-shallow junctions (USJs) in the source/drain extension regions. The problems of transient-enhanced diffusion (TED) and electrical de-activation [1, 2] are of particular concern. TED of n-type dopants may occur during annealing, causing the depth of ultra-shallow junctions to become deeper. In order to prevent diffusion, we must control the condition of implantation and annealing precisely.

Germanium was the first semiconductor used at the dawn of semiconductor technology, but due to the instability of the oxidation layer and lack of high temperature enduring characteristics, it is quickly being replaced by silicon. The oxidation layer problem is irrelevant when high-k materials are employed instead of SiO_2 [3]. One of the key technologies for the oxidation layer, which is formed at low temperatures, was using atomic layer deposition, making Germanium transistors gain renewed attention. One of reasons why Ge has attracted attention again is the higher mobility of Ge than Si. The mobility of holes and electrons in Ge is 1900 and 3900 cm^2/Vs, respectively. Both of them are higher in mobility than Si. Furthermore, the International Technology Roadmap for Semiconductors (ITRS) predicts that germanium would replace silicon for channels beyond 10 nm node transistors. Therefore, studying germanium transistors is an important trend in the future.

The n-type dopants in Ge can't be activated sufficiently at low-temperature annealing. Large amounts of impurities from diffusion occur at high-temperature annealing, producing a serious short-channel effect on nano-size transistors. In order to overcome this challenge, low-energy microwave annealing (MWA) is used to activate the dopants in this study. In the past, various high-temperature annealing processes have been studied to electrically activate implanted

dopants and to repair lattice damage caused by ion implantation, and thus reduce junction leakage currents to retain the junction and contact resistances low. Even though many techniques show excellent activation behavior on source/drain annealing, there are some problems making the process more complex than required for improving device performance and shrinking junction depths simultaneously. Microwave annealing (MWA) is a good technique for low-energy annealing and a longer processing period. Annealing energy levels will affect the ability to repair the lattices, whereas sufficient annealing time will recrystallize completely. MWA is a process that heats materials by bombarding it with electromagnetic radiation in the microwave spectrum, causing polarized molecules in the material to rotate and build up thermal energy. The most important purpose of the low-energy MWA process is to effectively repair destroyed lattices and to activate the dopant-ions without dopant diffusion [4-7]. The heating level of MWA energy is lower than traditional heating levels. The accurate measured temperatures of MWA are shown in Fig.1 during various heating energies: 1P (0.6 kW) to 2.5P (1.5 kW). The real measuring time is longer than the real operation of the MWA machine. For the energy of one power, the actual temperature is lower than 270°C, and the line is straight because the infrared thermometer we used can't measure lower than 270°C. For the energy of 2P, the peak temperature from the curve is ~430°C. For the energy of 3P, the peak temperature from the curve is ~490°C. After measuring the actual temperature, we have proved that the heating level of MWA is lower than traditional annealing methods.

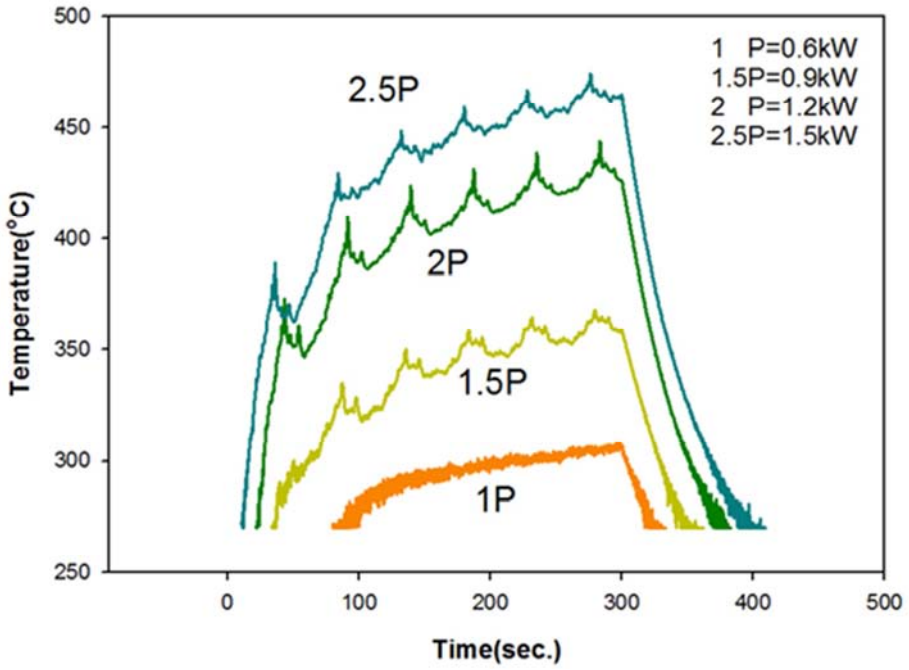

Figure 1. *The temperature profile of MWA with different power energy.*

The heating way of MWA is more uniform than traditional methods. The microwave field is usually non-uniform, and localized superheating occurs due to the design of traditional microwave ovens. In this paper, the MWA machine which we use has been presented to improve the uniformity of previous paper [8-10].

The heating reaction of MWA is focusing, and the reaction regions (such as SPER, activation, et al.) can be separated. MWA technology can also apply to the fabrication of Ge-based MOSFET [11]. Two-step MWA in different powers was employed to anneal the implanted Ge wafer. We used high energy 1.5P (0.9 kW; ~350°C) - 2.5P (1.5 kW; ~460°C) in the first-step of MWA to accomplish the solid state epitaxial recrystallization (SPER) completely. In the second step, we use gentler and lower energy MWA, 1.5P (0.9 kW; ~350°C), instead of traditional high-temperature annealing, to activate the dopants efficiently and achieve low sheet resistance. A superior diffusion limitation is realized without de-activation in this study, and the sheet resistance is lowered to 78 Ω/sq, and the activation level is raised to10^{20} cm^{-3}, which can apply to our device.

2. Experimental Procedure

Commercially available (100) p-type Ge wafers were used, and they were cleaned using a standard RCA process. Then the wafers were implanted using $^{31}P^{+}$ (10 keV, @1E15 atoms/cm^2) at 150°C. Using a high implantation temperature can help to repair any damages during implantation, but it can't completely recrystallize the lattices. A 150 nm thick silicon dioxide (SiO_2) layer was deposited on the sample, and this has been shown to suppress Ge surface oxidation and hence prevent Ge surface loss during annealing [12]. The first-step, MWA at 1.5P (0.9 kW)–2.5P (1.5 kW) for 75 s, was employed

to anneal the Ge samples to find the best condition for SPER. The second-step of MWA, at 1P (0.6 kW) and 1.5P (0.9 kW) for 100–600 s, was studied after the first-step's annealing. After annealing, the samples were then etched in a buffered hydrofluoric acid (HF) solution to remove the SiO_2 layer. A buffered HF solution etching has been shown only to etch the silicon dioxide capping-layer and not affect the underlying Ge layer [12]. The dopant-activation situation was analyzed by TEM, Four Point Probe, Hall measurement, and Raman spectrum. Four Point Probe was used to investigate the characteristics of dopant activation or de-activation. Resistivity, carrier concentration, and mobility were measured using the Hall measurement. The Raman spectrum was used to characterize the crystal structures of the implanted samples before and after annealing.

In the end, we fabricated a simple MOS device of planar structure to analyze the performance by the drain current-gate voltage characteristics. The process flow of the simple n-MOS device is shown in Fig. 2. To manufacture the n-MOS planar structure, the activation patterns were defined on a (100) p-type Ge wafer, and the gate oxide (Al_2O_3) thinkness was formed 5 nm using ALD at 320°C. TiN was then deposited 50 nm by PECVD as the metal gate electrodes. Gate region was defined by the lithography and etching steps. The next step was to form the spacer, and then the source and drain were implanted with $^{31}P^+$ (10 keV, @1E15) at 150°C. Finally, the two-step MWA was adopted to activate the source and drain region. The characteristics of the resulting devices were examined by measuring the drain current-gate voltage ($\log I_{ds}$–Vg) characteristics.

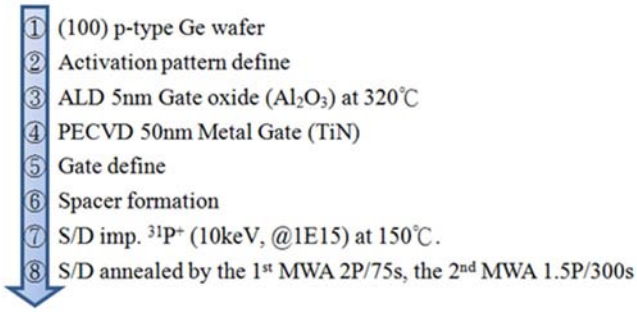

Figure 2. *Process flow of simple n-MOS device fabrication.*

3. Results and Discussion

In order to recover the destroyed lattices completely and to achieve solid phase epitaxial recrystallization (SPER) after annealing, different MWA energies were applied. Figure 3 shows the sheet resistances of P implantation (10 keV, @1E15) at 150°C after MWA 1.5P (0.9 kW) -2.5P (1.5 kW) for 75 s. We can observe that the lower sheet resistance is located at MWA 2P, which is about 193 ohm/sq. It displays that the heating level of MWA 1.5P is not able to repair the damages to obtain SPER. After annealing at 2.5P, the sheet resistance increases because de-activation may occur. We infer that the annealing condition of MWA 2P for 75 s is enough to recover the destroyed lattices and to repair the damages to obtain SPER.

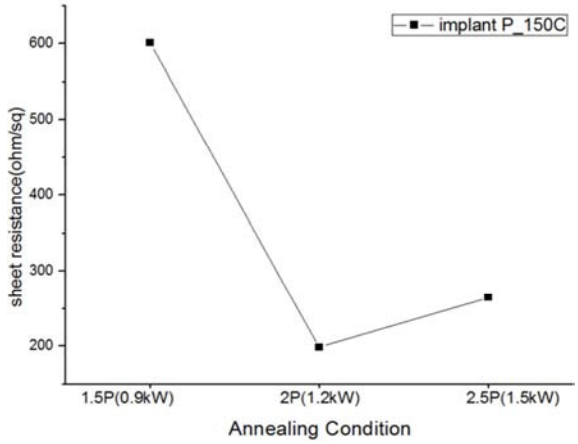

Figure 3. *Sheet resistance of P implantation (10 keV, @1E15) at 150°C after different energy MWA for 75 s.*

Figure 4 is the thickness of the amorphous layer from TEM cross-sectional images on the implanted-P (10 keV, @1E15) at 150°C, which is annealed at 1.5P and 2P for 75 s. As-implanted Ge sample from Fig. 3 (a) shows a 23 nm amorphous layer which is caused during the implantation process. Although the high implantation temperature is able to help to repair the damages during the period of implantation, the amorphous layer is still exists, which is caused by high speed ion bombarding. Figure 3 (b) shows this sample after annealing at MWA 1.5P for 75 s, and the amorphous layer merely remains at about 7 nm. Furthermore, after annealing at MWA 2P for 75 s, there is no amorphous layer left, as shown in Fig. 3 (c). This illustrates that this annealing condition of MWA at 2P for 75 s shows excellent recovery and recrystallizing ability.

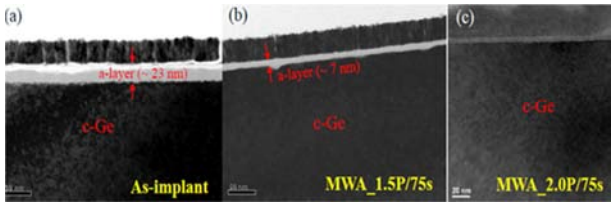

Figure 4. *The TEM cross-section images of the P-implanted Ge and which is annealed after 1.5P to 2P for 75 s.*

Figure 5 shows the Hall Effect results on carrier concentration, Hall mobility, and Resistivity of P (10keV, @1E15) at 150°C, annealed at MWA 1.5 to 2.5P for 75 s. From the trends of the Hall results, we can verify the sheet resistances and TEM results. The MWA 1.5P is insufficient to repair the destroyed lattices. The MWA 2P is enough to achieve SPER because carrier concentration and mobility increase, whereas the resistivity decreases. In general, when carrier concentration increases, mobility decreases. But in this Ge case, the carrier concentration increases while mobility also increases. This infers that mobility is dominated by ionized impurity scattering. When elevating energy, electrons move faster and are influenced little by Coulomb's law, so mobility increases. After annealing at MWA 2.5P, de-activation takes place due to the clustering of phosphorus interstitials. While the higher power MWA of 2.5P (1.5kW) is

employed, the de-activation reaction is stronger than the activation. The carrier concentration decreases and resistivity increases slightly because of the de-activation reaction. Mobility decreases because the phonons vibrate drastically in the higher energy and it would block the electrons moving.

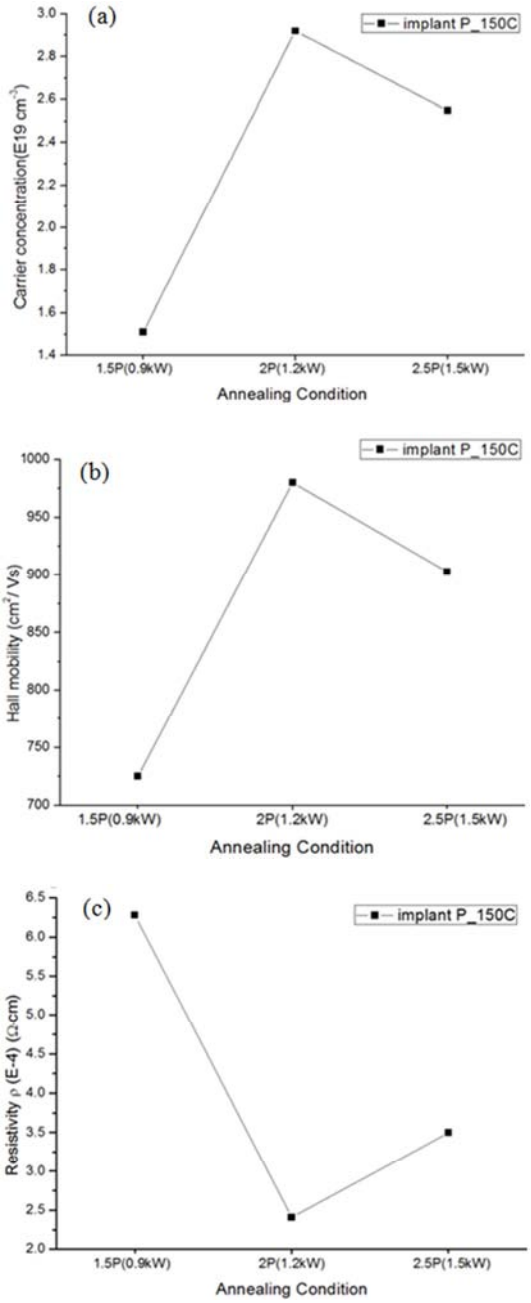

Figure 5. *The Hall Effect results on (a) Carrier concentration, (b) Hall mobility, and (c) Resistivity of the implanted samples after MWA 1.5P to 2.5P.*

The Raman spectrum was applied to analyze the implanted samples after MWA, shown in Fig. 6. From the spectrum, the bulk Ge sample is dominated by an intense Ge-Ge first-order optical phonon mode near 300 cm^{-1}, and the "weak hump" second-order transverse optical (TO) phonon mode is near 570 cm^{-1}. After ion implanting P at 150°C, the Raman spectrum shows a random profile that does not form in the crystal Ge phase. The spectrum of the samples after MWA 1.5P shows no recognizable peak around 570 cm^{-1}. In contrast, the spectrum of the samples after MWA 2P has an obvious peak like bulk Ge. It illustrates that the annealing condition at MWA 2P for 75 s has great recovery and recrystallization, and that the Ge layer is rebuilt more effectively.

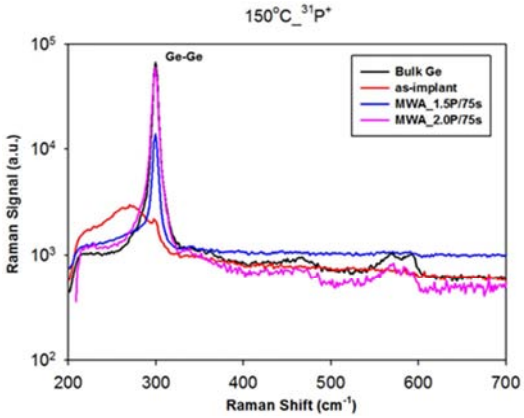

Figure 6. *Raman spectrum of bulk Ge, P-implanted at 150°C and annealed by MWA at 1.5P and 2P for 75 s*

The first-step MWA with 2P (1.2 kW) for SPER is not enough to attain dopant activation, and thus the second-step MWA is carried out. In this second step, we use lower-energy microwaves of 1P (0.6 kW) and 1.5P (0.9 kW), and the annealing times were employed from 100 s to 600 s. Figure 7 shows the sheet resistances of P-implanted Ge before and after two-step MWA. The sheet resistance of the one-step MWA at 2P for 75 s is ~193 ohm/sq, which has good recovery and recrystallization, as mentioned above. The sheet resistances of the second-step MWA samples decrease as the annealing times increase. The lowest sheet resistance is ~78 ohm/sq, which is achieved with 2P for 75 s in the first-step MWA and 1.5P for 300 s in the second-step MWA. But the sheet resistances rise after the second-step MWA for 600 s because of de-activation. This indicates that using a lower-energy microwave in the second step to anneal P-implanted Ge samples, which has already been SPER by the first-step MWA 2P, can decrease the sheet resistances effectively.

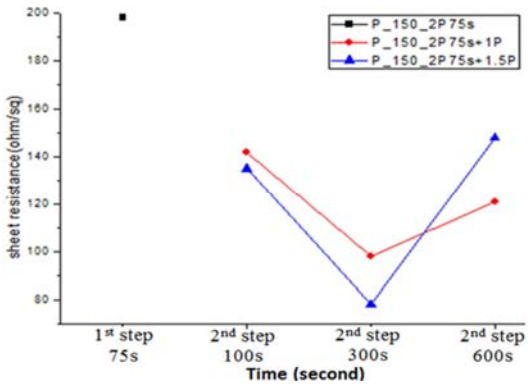

Figure 7. *The sheet resistance of P-implanted and annealed by the first-step MWA and the second-step MWA for different times.*

Figure 8 shows the Hall Effect results on Hall mobility and carrier concentrations of the annealed samples. From the trends

of Hall mobility and carrier concentrations, we can observe that they correspond to Fig. 6. While the annealing time increases until 300 s, carrier concentration and mobility increase. The Hall mobility of the second-step MWA for 300 s is 1298 cm^2/Vs, whih the carrier concentration will rise to 1.025×10^{20} cm^{-3}, which achieves our target dopant activation level of 10^{20} cm^{-3}. This indicates that the value of the first-step MWA 2P for 75 s and the second-step MWA 1.5P for 300 s has the best performance with excellent activation. SPER and activation couldn't be achieved without de-activation in the meantime with the one-step MWA. High-energy and short-time MWA is employed in the first step to repair the lattices and achieve SPER. Low-energy and long-time MWA is used to accomplish dopant activation in the second step.

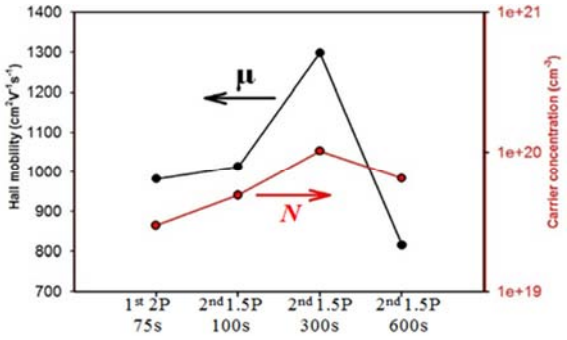

Figure 8. *The Hall Effect results of P-implanted Ge, annealed first by MWA 2P for 75 s and the second-step by MWA 1.5P for 100 s to 600 s.*

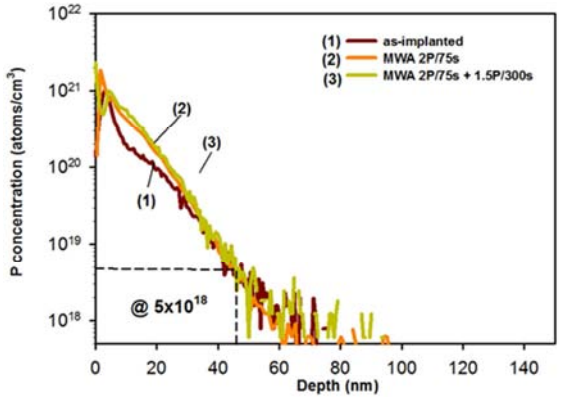

Figure 9. *The SIMS profiles of P-implanted Ge, annealed before and after two-step MWA.*

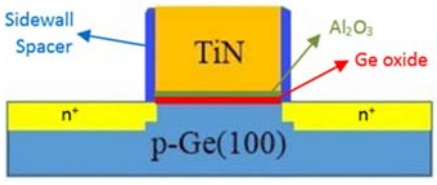

Figure 10. *n-MOS device structure on using (100) p-type Ge.*

Figure 9 shows the SIMS profiles of P-implanted Ge, which is annealed first by MWA 2P for 75 s and the second-step by MWA 1.5P for 300 s. The junction depth defined at a background concentration @5E18 is about 43 nm. In these profiles, we can see the diffusion depths of the one and two-step microwave annealed samples. They are similar to the diffusion depth of the as-implanted sample, and this indicates that there is almost no phosphorus diffusion after MWA, which illustrates that the diffusion control of MWA regardless of one and two steps is fine.

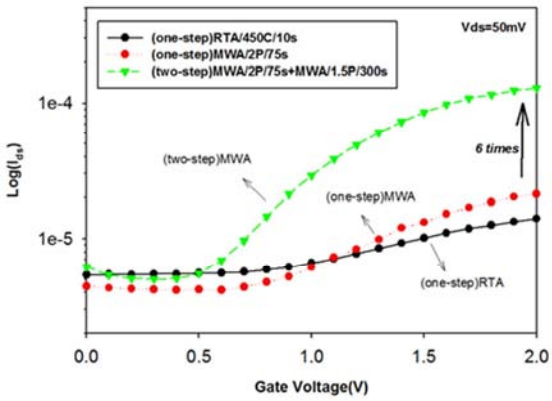

Figure 11. *The drain current-gate voltage (log I_{ds}–Vg) characteristics of n-type MOS on the Ge substrate with the TiN (50 nm) / Al_2O_3 (5 nm) / GeOx / Ge gate stacks.*

In the end, we fabricated a simple typical device of planar structure by using new material bulk Ge to realize the characteristics of MOS. The planar structure is schematically shown in Fig. 10. First, a 200 nm silicon dioxide field oxide layer was deposited on p-type Ge (100) wafers. Second, the active region was defined for a source/drain pattern by lithography process. Third, a thin film Ge oxide was grown for gate oxide because many recent studies have revealed that Ge oxide interfacial layers can provide superior MOS interfaces with lower interface state density (Dit) among the various Ge MOS interfaces [13]. And then, Al_2O_3 by ALD at 320°C for 5 nm was formed to be the gate stack insulator. Here, in order to reduce the resistivity, a metal gate TiN was grown on an insulator oxide layer of 50 nm using PECVD. Next, the gate mask was used to define the gate using the second lithography process, and the useless region was removed by etching solution. A sidewall spacer was formed to protect the gate stack and to be the source/drain buffer layer. The following step was to ion implant the source/drain region by injecting $^{31}P^+$ (10 keV, @1E15 atoms/cm^2) at 150°C. Finally, we conduct a one-step MWA at 2P for 75 s and the second-step MWA 1.5P for 300 s in comparison with the traditional annealing method of RTA at 450°C for 10 s.

Figure 11 shows the drain current-gate voltage (log I_{ds}–Vg) characteristics of n-type MOS with the TiN (50 nm) / Al_2O_3 (5 nm) / GeOx / Ge gate stacks under an EOT (equivalent oxide thickness) of 1.5 nm. The usual operation of n-type MOS devices can be confirmed from the drain current–gate voltage characteristics. The measurement drain voltage Vds is 50mV, and the channel width /length is 10 μm /10 μm. The on/off current ratios and the subthreshold swing factors of devices after different annealing conditions are shown in Table (I). The device with two-step MWA (2P/75 s + 1.5P/300 s) shows very promising results, including the smallest S. S. factor (~ 900 mV/ dec), and the highest $I_{on/off}$ ratio (~2.6×10^1).

We have demonstrated that the characteristics of the device in using two-step MWA are better than those of only one-step MWA and RTA devices.

Table 1. *List of the ($\log I_{ds}$–Vg) characteristics of n-type MOS on the Ge substrate.*

Annealing condition	SS(mV/decade)	$I_{on/off}$
RTA at 450°C for 10s	>1000	$< 10^1$
MWA at 2P for 75s	>1000	$< 10^1$
MWA at 2P for 75s + MWA at 1.5P for 300s	~ 900	$\sim 2.6 \times 10^1$

The higher on/off current ratio brings a better switching function. It is easier to distinguish the on/off switch obviously. Subthreshold Swing (slope) is defined to be the inverse slope of the ($\log I_{ds}$ –Vg) characteristic in the subthreshold region. The smaller S. S. factor represents that the gate has greater control on subthreshold current. If the S factor is small, the leakage current will be smaller during device operation. Smaller S factor also indicates that the interface defects will reduce. Previous literature [13] mentions that n-MOSFETs with the HfO_2 (2.2 nm) / Al_2O_3 (0.2 nm) / GeOx (0.35 nm) / Ge gate stacks under an EOT of 0.76 nm have on/off current ratios of 10^3 and S factors of 80 mV/dec. In the future, we will research how to improve the performance of the Ge n-MOS device with two-step MWA.

4. Conclusion

This study has proved that the two-step MWA with two different energies has excellent performance for achieving SPER and dopant activation in P-implanted Ge. In the first-step MWA, the TEM images show that the energy of 1.2 kW for 75 s can repair the amorphous layer caused by implantation to crystal state completely and to realize SPER effectively. After the second-step MWA with low-energy at 0.9 kW for 300 s, the sheet resistance lowers to 78 ohm/sq, the Hall mobility increases to 1298 cm^2/Vs, and carrier concentration even reaches up to 1.025×10^{20} cm^{-3}. This illustrates that the two-step MWA can attain dopant activation without de-activation effectively, which is suitable in forming our devices. The ($\log I_{ds}$–Vg) characteristic curves show that the device annealed by two-step MWA has the better characteristics than only using MWA or RTA. The S. S. factor is 900 mV/dec, and the $I_{on/off}$ ratio rise to 2.6×10^1. This has demonstrated that the two-step MWA has excellent control, significantly regarding leakage current.

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