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A Compact Model of Mosfet Transistors Including Dispersion and Thermal Phenomena

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Abstract: This paper propose a new electro-thermal model nd presents a method of studying the thermal phenomena in power MOSFET transistors, utilizing Advanced Design System techniques by a Symbolic Defined Device (SDD). The model incorporates the thermal effects and the temperature evolution in the device and captures the heat dissipation from the silicon chip to the ambient air by providing three thermal capacitances and three thermal resistances (thermal network). It enables a better estimation of the device's reliability and lifetime. Furthermore, it can be used to make a connection between the electrical parameter drifts and the existing failures types. The developed model reflects superior performance in terms of accuracy and flexibility and the results obtained indicate a good agreement with the operating conditions.

Keywords: Modelling, Electro-Thermal, Power MOSFET, Temperature, Self-Heating, Thermal Network

1. Introduction

Electrical characteristics of semiconductors are sensitive to changes in temperature, in particular power devices. The study device is used in different application areas; like telecoms (base station), radars and space activities. The continuing trend towards devices miniaturization makes the consideration of the thermal aspects very critical, both in the design and operation [1-2]. The technology evolution puts stringent requirements on performance and hence requires powerful characterization and simulation tools that can adequately assess the quality and reliability of the produced devices in different operating modes.

We present an electro-thermal model capable of evaluating the temperature effects of a power MOSFET. The temperature effects can limit the lifetime of MOSFETs and play an essential role in the failure mechanisms [3-5]. These effects have been satisfactorily modelled in previously works by Miller et al [6], based on analytical expressions, and by Angelov et al [7] Chalmers model. In this paper we present an electro-thermal model capable of capturing the thermal dependencies and yields superior performance in terms of modelling accuracy and flexibility.

This paper is organized as follows: Section II describes our electro-thermal model. The results and discussion are presented in Section III. Conclusion and perspectives are given in Section IV.

2. Electro-thermal Model

By capturing the thermal dependencies of the power MOSFET our modelling approach can provide a fuller characterization that evaluates the electro-thermal interactions during operation at different levels of the component (silicon chip to the ambient air). An empirical non-linear model is shown in Figure 1. This was implemented using the symbolic device (SDD) in the ADS software.

The power MOSFET model is composed of several passive linear and non-linear components, non-linear drain-source current generator dependent on gate-source and drain-source voltages and a thermal circuit as shown in Figure 1.

The current model of proposed channel is formulated as follows [8-9]:

$$I_{ds} = Beta \cdot \left(V_{gm}^{Vg\exp}\right) \cdot \left(1 + Lambda \cdot V_{ds}\right) \cdot \tanh \cdot \left[\frac{\left(V_{ds} \cdot Alpha\right)}{V_{gm}}\right]$$

$$\cdot\left[1+k_1\cdot\exp\left(V_{breff1}\right)\right] \quad (1)$$

The thermal network is a low-pass filter with the total thermal resistance R_{th} correlated with static characteristics (chip-ambient air). The total heat capacity C_{th} represents the dynamic characteristics of the heat flow inside the transistor. The static temperature of the channel may be written as below: [10]:

$$\Delta T = R_{th}\cdot P_{diss} + T_a \quad (2)$$

$$P_{diss} = I_{ds}\cdot V_{ds} \quad (3)$$

Where ΔT is the junction temperature, P_{diss} is the instantaneous total power absorbed in the transistor, and T_a the ambient temperature. R_{th_CP}- the thermal chip-package resistance (a technological characteristic specific to a transistor and given by the manufacturer), R_{th_PH}- the thermal package-heat sink resistance (referring to a conduction transfer; this resistance can be decreased by improving the contact between the package and the heat sink surface, by using silicone oil), R_{th_HA}- the thermal heat sink-ambient air resistance (depending not only on the size, form and structure of the heat sink, but also on its orientation and on the air stream flowing around it).

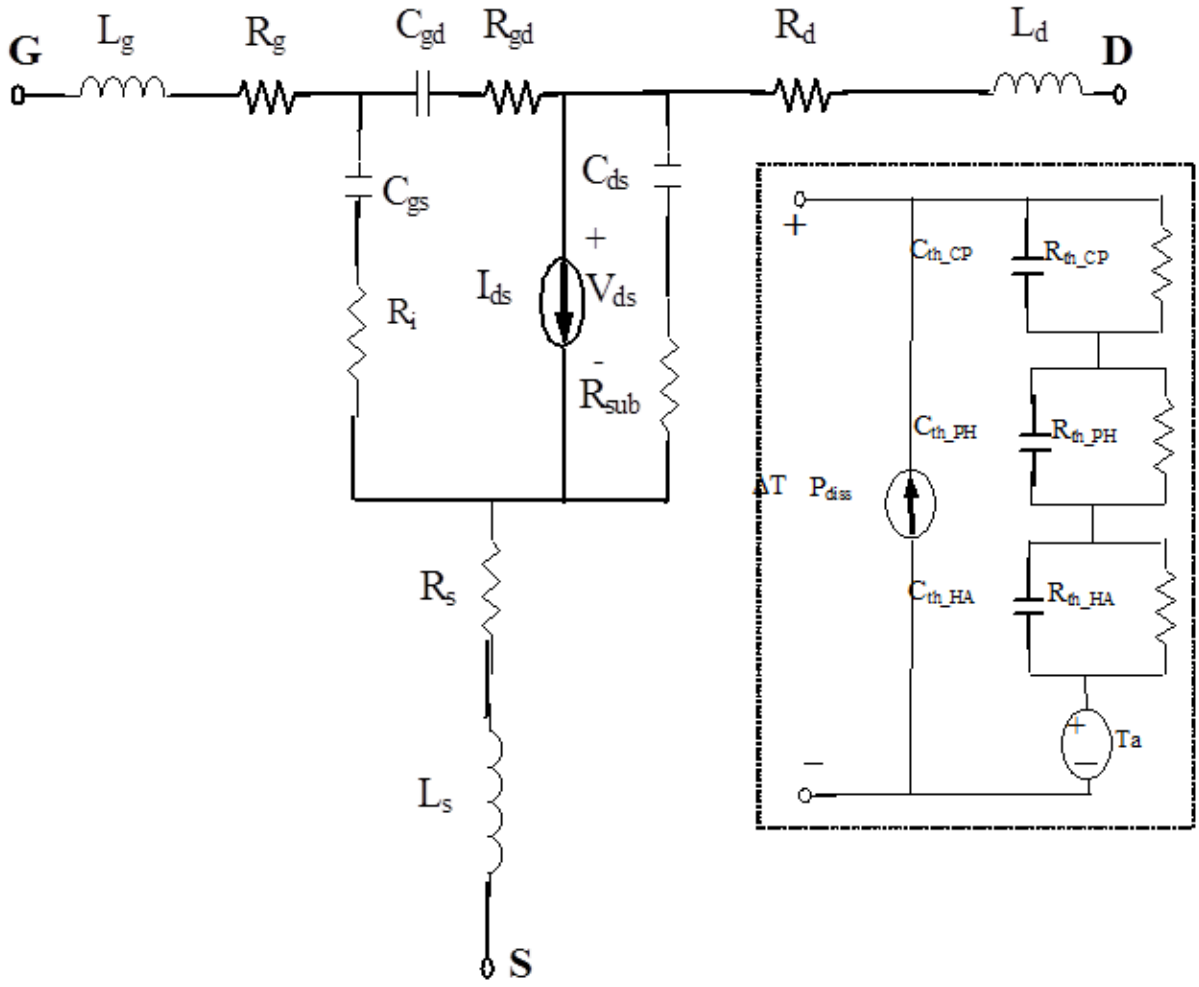

Fig. 1. *Large-signal equivalent circuit of power MOSFET model with a thermal network.*

Non-linear functions of capacity C_{gs} (gate-source), C_{gd} (gate-drain) and C_{ds} (drain-source capacitance) are used in this model with linear temperature dependence [6]:

$$C_{gd}\left(T\right) = \left[C_{gd1} + \frac{C_{gd2}}{1+C_{gd3}\cdot\left(V_{gd}-C_{gd4}\right)^2}\right]\cdot\left(1+C_{gdT}\cdot\Delta T\right) \quad (4)$$

$$C_{ds}\left(T\right) = \left(C_{ds1} + \frac{C_{ds2}}{1+C_{ds3}\cdot V_{ds}^2}\right)\cdot\left(1+C_{dsT}\cdot\Delta T\right) \quad (5)$$

The electro-thermal model will be used as a reliability tool that facilitates linking the change in the transistor electrical parameters (after accelerated aging tests at different temperatures or functioning) and the degradation phenomenon.

3. Results and Discussions

Fig. 2 (line) shows the instability and the thermal runaway which occurred due to temperature effects. To limit and decrease this problem and to improve the measurement conditions, a solution which proves to be a precious working tool would make it possible to thermal protects the component. It consists of mounting the component on a heat dissipator. Thanks to this solution, we can obtain more thermally stable measurement conditions (Fig. 2, dashed). The importance of cooling systems like the heat sink and the Peltier module could be observed.

The model of Figure 1 was implemented using the symbolic defined device (SDD) in ADS software. The results obtained are discussed next.

Fig. 3 shows the variations of the channel current from the transistor output characteristic with changing parameter values (Alpha, Beta and V_{br}). Each parameter has a unique role in describing the channel current, with a slight interdependence between them. The different parameters play on the shape in order to fit the measured curve.

The I-V characteristics of the transistor in various conditions (chip, package, heat sink) and the fitted results are in good agreement, as has been presented in Fig. 4.

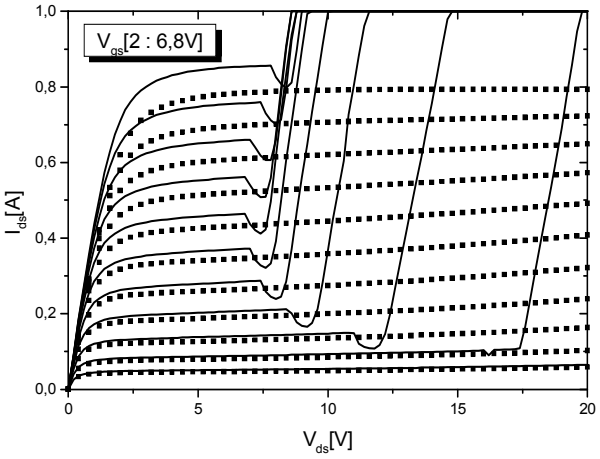

Fig. 2. *Output characteristics: Thermal instability effect (line) and stable temperature conditions (dashed).*

Figure (5) shows the channel current variation at different temperatures. It is evident that channel current I_{ds} vary linearly with temperature at low current levels. This is due to the threshold voltage reduction [11].

Indeed, for a MOSFET, the current relative dependence on temperature is linked to two contradicting phenomena. The current I_{ds} is proportional to the mobility μ and to the electrons concentration in the n-channel [12]. When the temperature increases, n increases while μ decreases. For low current values, the decrease effect in mobility is negligible compared to the increase in the bearer's number and thus, the current value increases [13]. On the other side, when the current value is important (high current level), the mobility effect becomes dominant, hence resulting in a decrease in current with temperature [11] [14].

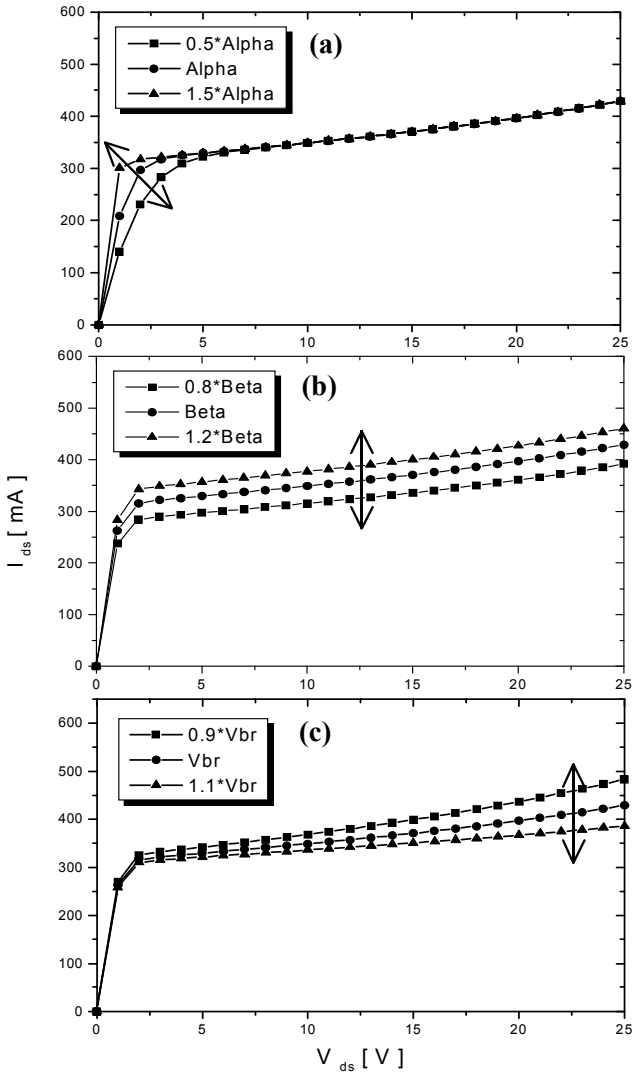

Fig. 3. *Calculated channel current variation versus drain voltage with varying parameter values for: (a) Alpha, (b) Beta and (c) Vbr.*

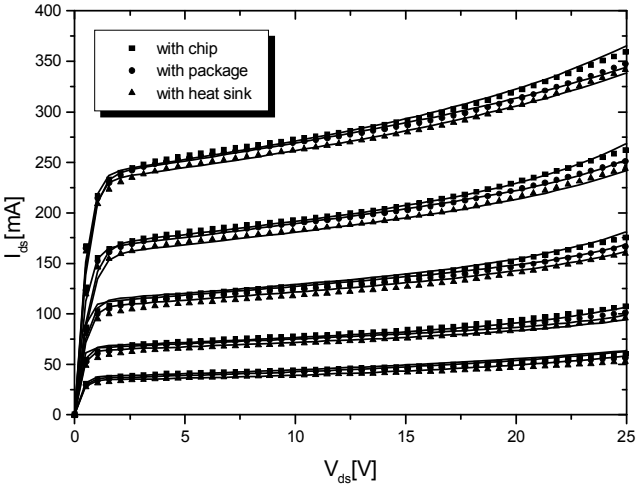

Fig. 4. *Measured (dashed) and modelled (line) output characteristic with various conditions, Vgs=[3: 6V], step=600mV.*

A more detailed study on the effects of the MOS physical and technologic parameters shows that the threshold voltage

decreases with temperature [6]. This variation with temperature is linear and can be represented as follows [6]:

$$V_t = V_{T0} + (V_{tT} \cdot T_j) \quad (6)$$

Where T_0 is the ambient temperature, V_{T0} is the threshold voltage at T_0, V_{tT} is the coefficient of the equation and T_j is the junction temperature.

The threshold voltage is a parameter strongly dependent on temperature, as shown in Figure 6, and affects the performance of the power MOSFET. We note that the threshold voltage decreases with temperature. The change of this voltage is mainly caused by the change of Fermi potential Φ_F with temperature [12].

The temperature effect was observed and modelled, as shown in Figure 7. It occurs and increases when a voltage is applied to the device [10]. The channel current is proportional to the drain voltage and gate voltage. This illustrates the consistency of our electro-thermal model as any additional current passing in the transistor yields a significant increase in temperature.

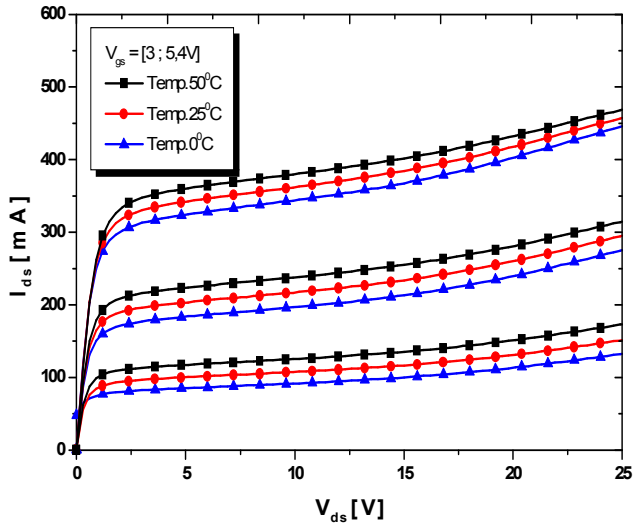

Fig. 5. Variation of low levels of channel current at different temperatures.

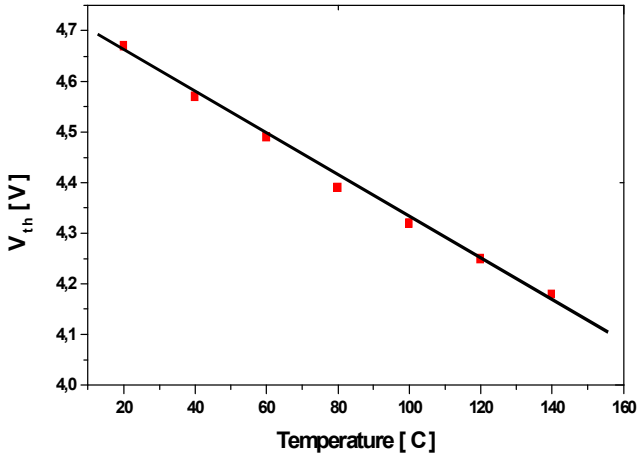

Fig. 6. V_{th} variation as a temperature function.

The resistance in the conducting state, which we believe, is defined by the ratio of drain voltage to the drain current linear [12], and is inversely proportional to the later.

$$R_{ds\_on} = (V_{ds} / I_{ds})_{V_{ds \to 0}} \quad (7)$$

The expression for the instantaneous junction temperature of the transistor was developed by making use of the existing duality between heat transfer and electrical phenomena summarized in Table 1. The main significant parameters of the model are shown in Table 2.

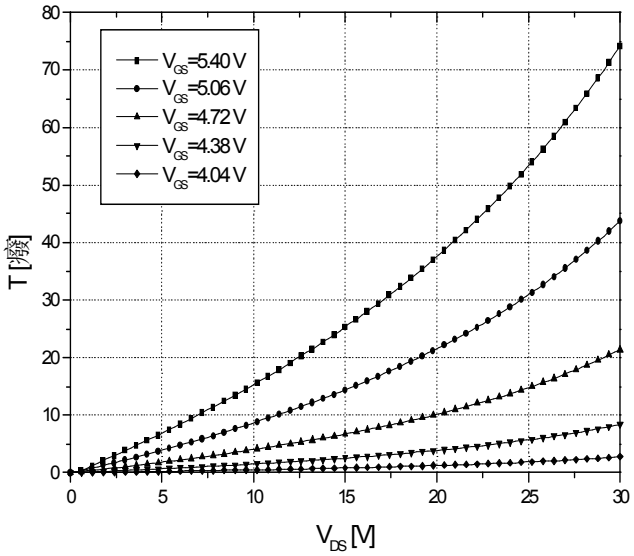

Fig. 7. Simulation of the temperature evolution inside the component.

The on-resistance decreases when the gate-source voltage increases [15]. The parameter R_{ds_on} is dependent on the distribution and dissipation of heat, which represents the heat flow in the transistor [10]. It also reflects the different values of the junction temperature. We note that R_{ds_on} decreases with temperature in the case of low polarization (low value of V_{gs}), and increases for high polarizations [15].

The C-V characteristics of the transistor in various temperatures and the fitted results form IC-CAP plot optimiser are in good agreement, as presented in Fig. 6 and 10.

The figure 10 shows the modelling feedback capacitance (C_{rss}) at different temperatures. It is deduced from the intrinsic capabilities with the following combinations [12]:

$$C_{iss} = C_{gd} + C_{gs} \quad (8)$$

$$C_{oss} = C_{gd} + C_{ds} \quad (9)$$

$$C_{rss} = C_{gd} \quad (10)$$

The final result of dynamic modelling is illustrated in Figures 8,9 and 10, where the superimposition is very good (error rate lower correlation to 2%).

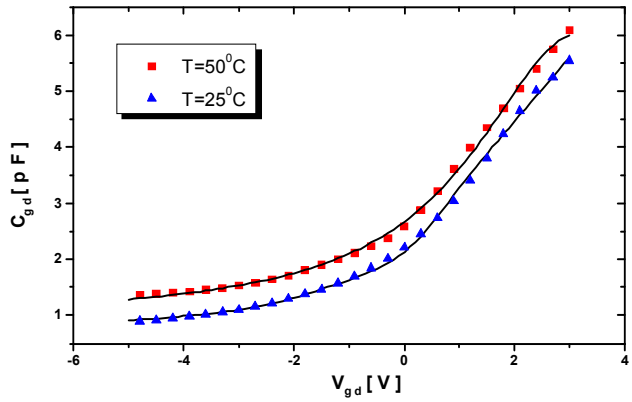

Fig. 8. *Gate-drain capacitance at different Ta, with Freq=1 MHz: Measured (dashed) and modelled (line)*

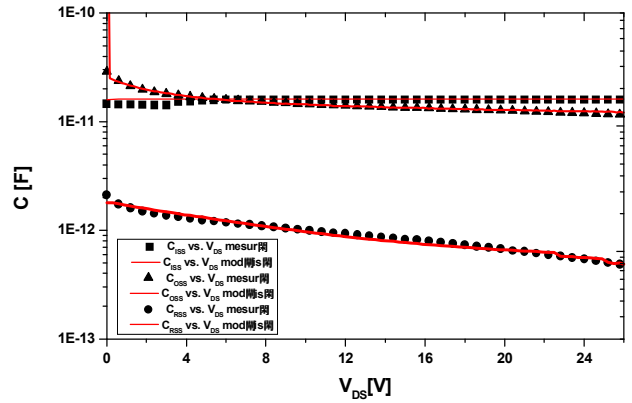

Fig. 9. *C_{ISS}, C_{RSS} and C_{OSS} capacitances measured (dashed) and modelled (line) for V_{DS} = 0 V-26 V, with Freq=1 MHz.*

The simulation results show good dynamic performance prediction of MOS device at different temperatures. Physically, the variation of that could be explained by the effect of the temperature on the Fermi level, which affects thereafter the width of the space charge zone and induces the variation of capacitance value.

Table 1. *Thermal and Electrical quantities equivalence.*

	Thermal quantity		**Electrical quantity**
P_{diss}	Power heat flow (W)	*I*	Current flow (A)
T_j	Temperature (K)	*V*	Voltage (V)
R_{th}	Thermal resistance (K /W)	*R*	Electrical Resistance (Ohm)
C_{th}	Thermal capacitance (J/W)	*C*	Electrical capacitance (F)

Table 2. *Model parameters.*

Parameter	**Definition**	**Unit**
Beta	Transconductance parameter	Siemens
V_t	Threshold voltage	V
Delta	Vt variation according to V_{ds}	V
V_{br}	Break down voltage	V
$K_{1/2,}$ $M_{1/3}$	Break down parameters	--
V_K	I_{ds} equation coefficient	V
Alpha	Linear range	1/Ω
Gamma	Slope of the channel current	--
Lambda	Shapes of the Ids saturation	1/V
V_{gexp}	Term of power	--

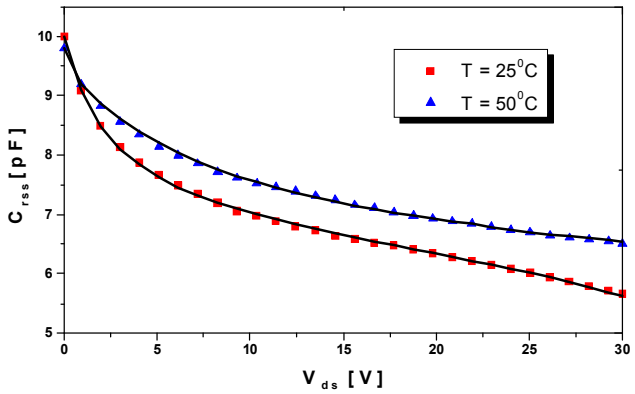

Fig. 10. *Crss capacitance at different Ta, with Vds= [0 V; 30 V] and Freq=1 MHz: Measured (dashed) and modelled (line).*

The integration of the electric field on all the thickness of the deserted zone gives the tension value of the barrier potential [16]:

$$V_b = q\left(N_A x_p^2 + N_D x_n^2\right) / 2\varepsilon \tag{11}$$

As we know that W = x_p + x_n:

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_b} \tag{12}$$

$$C_j(0) = \frac{\varepsilon S}{W} = \frac{\varepsilon S}{\sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_b}} \tag{13}$$

The deserted zone between the two conducting zones is similar to a plane condenser of S section (junction surface) such as shown in equation (13). When the operating temperature of the junction increases, E_g varies, therefore the height of the potential barrier decreases. Thereafter the capacitance increases.

Indeed, each defect type has activation energy i.e. a temperature from which it becomes active and acts on the device electric behaviour, and it has an important effect on the capacitance value [17-18].

In the last few days, we got the results of the temperature effect on the S-parameters and the evolution of electroma-gnetic interference in an application of static converters series chopper. Our aim is to make varying the junction temperature of the power transistor in the chopper circuit, while applying different temperatures to achieve a high junction temperature (T_j), which exceeds the value described by the constrictor. A test of the electromagnetic interference evolution will be determined.

4. Conclusion and Perspectives

The electric macroscopic parameters of the MOSFET (threshold voltage, channel current, transconductance $R_{ds\text{-}on}$, and capacitances) are highly sensitive to temperature variation.

The temperature increase can modify transistor behaviour and cause irreversible degradation of its performances. Therefore, the use of cooling systems is very essential to enhance measurement conditions of the device and to obtain better heat dissipation. Electro-thermal model that takes into account self-heating and the temperature effects has been developed for power MOSFETs. The model has been used to better understand the physical dynamics responsible of the degradation of performance. An increase in temperature can alter and degrade the transistor behaviour irreversibly, hence the importance of controlling the cooling systems and improving techniques for temperature measuring to better evaluate the thermal effects. Different levels of the system have been modelled successfully and the thermal dependencies have been properly captured. More heat cells can be added to better fit and reflect the heat dissipation in the device. Future work will focus on the S-parameters simulation for a complete compact model and studying the impact of temperature on electromagnetic interferences.

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