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Dynamic Comparator with Using Negative Resistance and CMOS Input Pair Strategies in F_S =4MHz-10GHz

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Abstract: A 4MHz-10GHz, 10ps/dec dynamic comparator with using negative resistance and CMOS input differential pair is proposed and designed in IBM 130nm CMOS process technology. In this design, we effort that taking maximum sampling frequency from CMOS technology and the proposed comparator consumes 110nw-146µW at 1.5V supply.

Keywords: Comparator, Negative Resistance, Optical Communication Systems, Transconductance Boosting, Dual-Rail Differential Input

1. Introduction

Generally, comparator is an important part of electronic systems, like Multi-GHz sample rate Analog-to-Digital convertors (ADCs) [1-4] as crucial components in optical communication systems. Due to limited accuracy, comparison speed and power consumption, comparison of the input data is regarded as one of the limiting factor of the high speed VLSI data conversion system. There is a growing need for the development of low power, low voltage and high speed circuit techniques and system building blocks because of increasing demand for portable and hand held high speed devices. On the one hand, low voltage operation is required to use as few batteries as possible for low weight and small size. On the other hand at the high frequency of operation, Low power consumption is demanded to prolong battery lifetime as much as possible [5, 6]. In the recent decade, due to the rapid advancement in Analog-to-Digital conversion devices, the rapid advancement of VLSI technology causes the evolution of digital integrated circuit technologies for signal processing systems that operate on a wide variety of continuous-time signals including speech, medical imaging, sonar, radar, consumer electronics and telecommunications.

Already with voltage scaling, sub-threshold voltage region demands require technology for new architecture and innovative circuits. Previous advances in MOS technologies meet it for higher speed applications, however due to MOS device mismatches, it is difficult to achieve a high speed and accuracy at the same time [7].

One of the key components in ADC as the fundamental block for the A/D conversion, are the comparators. In fact they are the link between analog domain and digital domain for compare a set of variable or unknown values against that of a constant or known reference value [8]. Many high speed ADCs demands high-speed, low-power comparators with small chip area. For low-voltage operation, developing new circuit structures is preferable in order to avoid stacking too many transistors between the supply rails [9]. The critical parameters in the ADC circuit design are speed, resolution, and power consumption. The ADC operates continuously, however processing digital signals are dependent on specific demands.

The organization of this paper is as follows. Section 2 described the proposed dynamic comparator. Section 3 illustrates the simulation results. A comparison to the conventional comparators is also presented, followed by the conclusions in section 4.

2. Proposed Dynamic Comparator

2.1. Structure

The comparators are consists of two parts namely pre-amplifier and latch that these parts operate in the same phase. Therefore, comparator can pull the latch. In the second phase, the pre-amplifier output nodes up to the power supply voltage level. Also, the comparator offset can be cancelled in

this phase [10-11]. Consequently, the comparator offset effect has not been considered in this paper. Fig. 1 shows the circuit diagram has been used in simulations that has been obtained from [12] with adding Q2 and Q4 that a dual rail pre-amplifier is achieved. For decreasing the loading effect on the comparator output, two CMOS inverters have been used to supply capacitive loads. The comparator consumes dynamic power because the comparator consists of dynamic latch and pre-amplifier [13].

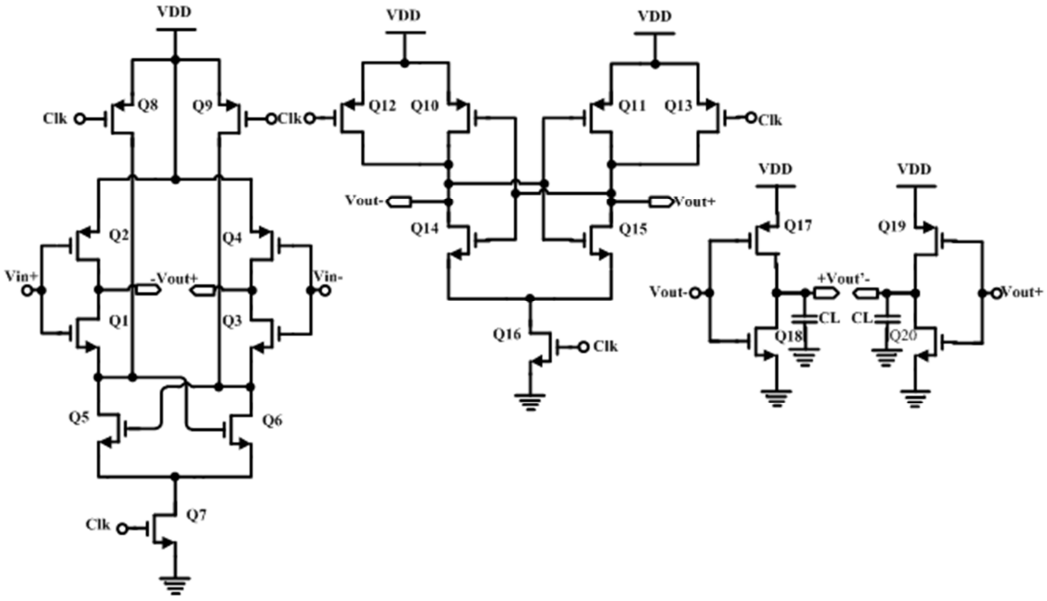

Fig. 1. *Schematics of the dynamic comparator and CMOS inverters.*

2.2. Transient Behavior

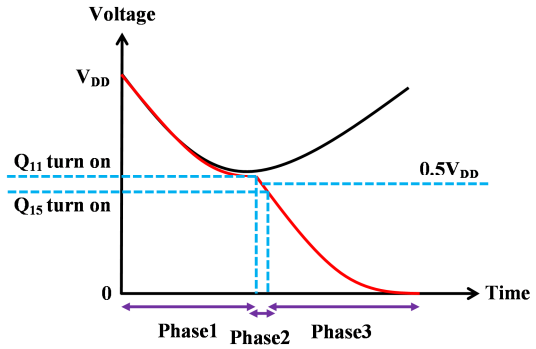

Fig. 2. *The sketch map for the transition behavior of the dynamic comparator.*

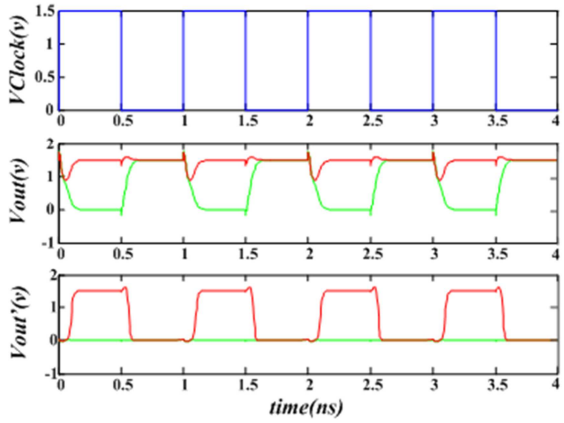

Fig. 3. *Simulated transient behavior of the proposed comparator structure.*

Fig. 2 shows the sketch map of the transient behavior of the dynamic comparator in the comparison phase. By the switching transistors Q8, Q9, Q12, and Q13 during the reset phase, the output terminals and the drain side voltages of Q5 and Q6 are all pulled high to VDD, respectively. By turning on the two tail transistors Q7 and Q16, the comparison phase begins. Therefore, the CMOS input stage transfers the differential small signal to the cross coupled stage. Q2, Q4 are activating when the input common mode is lower than the Q1 or Q3 threshold voltage. Therefore, the dual-rail differential input obtain since they are supplies the preamplifier output. Based on [14], the comparison transition can be divided into three phases (from phase 1 to phase 3). The output terminals are pulled down by two tail transistors Q7 and Q16 during the phase 1. Until one of the two output terminal voltages decreases to (V_{DD}-V_{thp}), the p-channel transistors Q10 and Q11 remain cut-off. The Q2 and Q4 activate when the cross-coupled stage composed from Q1, Q3, Q5 and Q6 cannot start. Therefore, the speed of proposed idea is more than paper [12]. In order to enhance the voltage difference between the output terminals, the cross-coupled inverters provide strong positive feedback in the phase 2.The transition state changes from phase 2 into phase 3 when one of the transistors Q14 and Q15 is cut-off. There is no static power dissipation since the current flows through these n-channel MOSFETs stop automatically after the transition. Fig. 3 shows transient behavior of the proposed dynamic comparator at 1GHz. As seen, both of the output terminals are pulled low in the beginning of the compare operation. One of the output terminals charge through the p-channel transistor when the transition goes from phase 1 into phase 2.

Therefore, the strong positive feedback provided by these

two cross-coupled inverters separates the output voltages. Against paper [12], this design aren't use from p-wells, thus the cost of comparator chip is lower.

3. Simulation Results

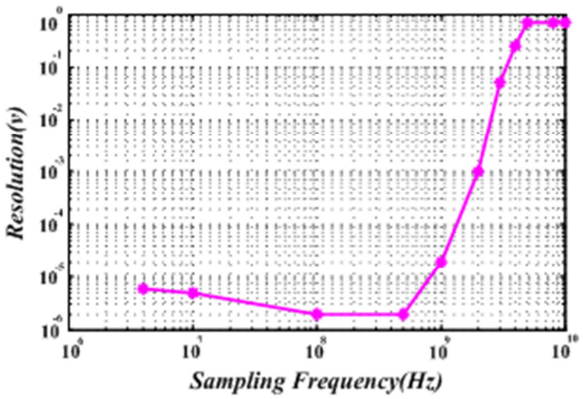

Fig. 4. *Simulated Resolution voltages versus Sampling Frequency at 1.5V supply voltage.*

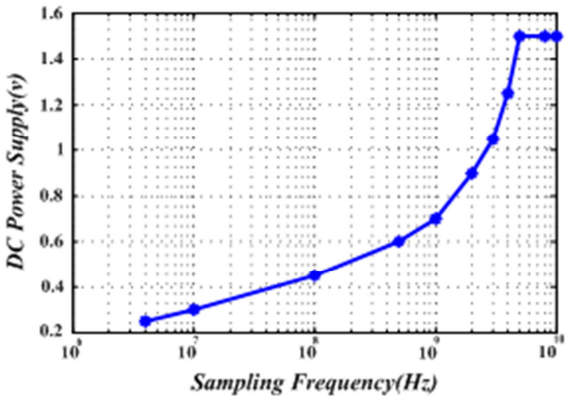

Fig. 5. *Simulated DC Power Supply versus Sampling Frequency.*

The comparator is designed in IBM 130nm CMOS process with 1.5V low threshold voltage device model (Vt≈0.3V). The resolution voltage (difference between input signals) versus sampling frequency is shown in Fig. 4. According to this Figure, resolution voltage is changing in range of 4MHz to 10GHz from 2μv to 700mv. The dc power supply versus sampling frequency is shown in Fig. 5. According to this figure, the minimum supply voltage is 250mv and maximum supply voltage is 1.5V. The power consumption versus sampling frequency is shown in Fig. 6. According to this figure, the minimum power consumption is 110nw at 4-MHz and maximum power consumption is 146μw at 10-GHz. According to simulation results, the delay versus CMOS differential input voltage (resolution) is shown in Fig. 7. The delay/log(ΔVin) in this figure is 10-ps/dec. Fig. 8 and Fig. 9 summarized the simulation results of delay and energy/decision versus input common-mode voltage, respectively. The delay of the proposed structure is also insensitive to input common-mode voltage (Vcm) that is the same as [15]. According to figure 8, the input common voltage is dual-rail because the range of common mode is between 0.1 to 1.1V. Therefore the proposed paper than papers [12] is very better. The energy dissipation is 2.5fJ/decision at Clk=1GHz and ΔVin=1.5V. That is very better than 71, 88 and 90fJ/decision in [12], [14]-[15], respectively. Table I summarizes the specifications of proposed dynamic comparator. We demonstrate that our comparator structure has the best delay/log (ΔVin) and energy/decision performance in comparison with recent publications [12], [14]-[16].

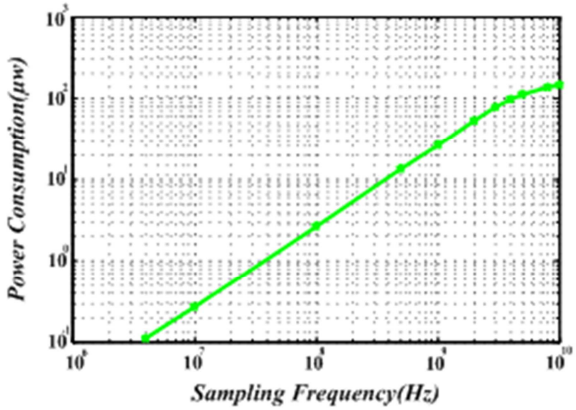

Fig. 6. *Simulated Power Consumption versus Sampling Frequency at 1.5V supply voltage.*

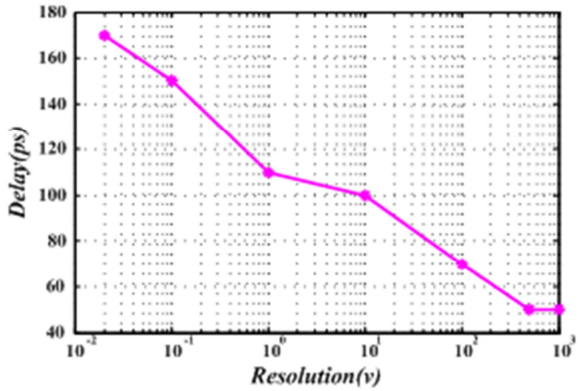

Fig. 7. *Simulated delay of different dynamic comparators versus differential input voltage. The delay is the time between clock edge and differential output signal of comparator crosses at 1/2 supply voltage.*

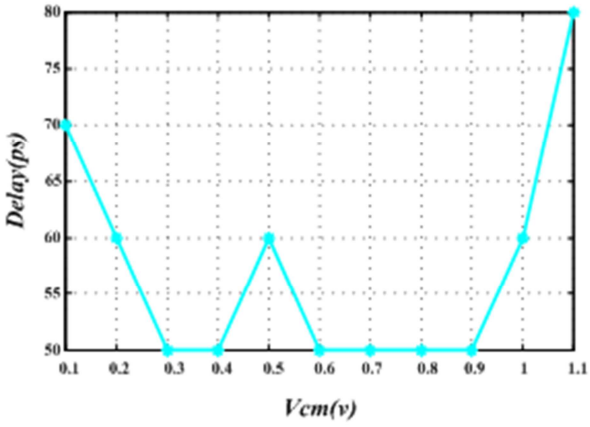

Fig. 8. *Simulated delay versus input common mode voltage at 1-GHz and 1.5V supply voltage.*

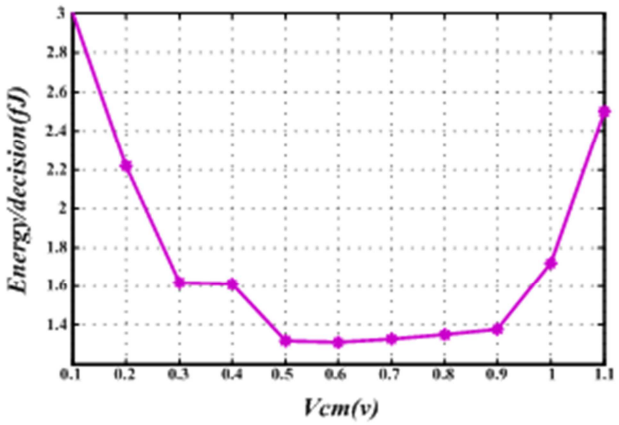

Fig. 9. *Simulated Energy/decision versus input common mode voltage at 1-GHz and 1.5V supply voltage.*

Table 1. *Performance summary and comparison This Work.*

Specifications	[12]	[14]	[15]	[16]	This Work
CMOS Process(nm)	90	Scaled to 90	90	65	130
Sampling Rate(GHz)	3	3	3	7	1
Delay/log(Resolution)	22	47	35	--	10
Supply/ICMV	1.2/1	1.2/1	1.2/1	1.2/1	1.5/1
Energy/decision(fJ)	71	88	90	185	2.5

4. Conclusions

The proposed dynamic comparator structure adds the CMOS input pair to negative resistance that causes the higher speed and range of V_{CM} of dynamic comparator at low power consumption. For receiving to multi-giga Hz in advanced deep sub-micron CMOS process in this design, the fingers of transistors increase that they achieve to minimum parasitic capacitance. Therefore this design received to highest sampling frequency in CMOS technology. In this paper, we received to delay/log (ΔVin) and Energy/decision equal 10 and 2.5fJ at 1GHz Respectively. Also in this paper, we received to sampling Frequency 10GHz at Resolution equal 1v.

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