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Experimental and theoretical study of parasitic effects in InAlAs/InGaAs/InP HEMT's

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Abstract: A detailed study of electrically active defects present in InAlAs/InP heterostructure and InAlAs/InGaAs/InP High Electron Mobility Transistors (HEMTs) grown by metal organic chemical vapor deposition (MOCVD) is presented. Current and capacitance Deep Level Transient Spectroscopy (I-DLTS and C-DLTS) techniques are used for the identification of active electrical defects. A notable correlation between deep levels observed by I -DLTS and C-DLTS results and the contribution of parasitic effects (Kink and Hysteresis effects) on output characteristics was evidenced. A new model for Kink effect is presented on InAlAs / InGaAs / InP HEMT's. This model uses a new polynomial dependence of sheet carrier concentration, on bias and temperature of device structure to calculate $I_{ds} - V_{ds}$ characteristics. The simulation model enables us to confirm that the Kink parasitic effect in $I_{ds} - V_{ds}$ characteristics is strongly correlated by trapping and detrapping mechanisms. Experimental and theoretical results obtained by the new model are in good agreement.

Keywords: DLTS, I-DLTS, I_{ds}-V_{ds}, PL, Kink Effect, HEMT

1. Introduction

A great progress has been made in the development of high performance InAlAs/InGaAs/InP high electron mobility transistors (HEMTs)[1]. These devices have demonstrated excellent performance at microwave frequencies for high temperature. InAlAs lattice matched on InP substrates is an attractive material for heterostructure and opto-electronic applications. Additionally, InAlAs has more advantages compared to InP with respect to device layer design due to its remarkably higher conduction band-edge discontinuity with InGaAs and a significantly larger band gap (1.42 eV versus 1.51 eV at 4K) [2].

One of the major issues that continue to limit the performance of InAlAs devices is the presence of electronic traps in the device structure. In InAlAs/InGaAs/InP HEMTs, the parasitic charge moving in and out of the traps on the surface and/or in the bulk of the heterostructure affects the density of the two-dimensional electron gas (2DEG) in the channel, causing effects such as current collapse [3, 4, 5], drain lag [6, 7], gate and light sensitivity [5] and transconductance frequency dispersion [8, 9]. The characteristic time of the recharging process in InAlAs ranges between nanoseconds and seconds, as a result, the trapping effects can limit device performance even at relatively low frequencies. In addition, the thermally activated traps contribute significantly to the device low-frequency noise [10, 11]. Recent active research turn about the minimization of these trapping effects because of their major contribution in the limitation of HEMT performances.

Another major factor that limits HEMT performance concerns defects related to technology process. These defects like dislocations cause significative

transconductance frequency dispersion [12, 13, and 14]. Most recent works in this microelectronics area concern the optimization of the InAlAs/InGaAs/InP structure process growth in order to secure the quality of device and circuit. These structures show the presence of several parasitic effects such as Kink and Hysteresis effect. Moreover, from the viewpoint of manufacturing, a means of eliminating or suppressing the Kink effect is necessary, but how this should be done is still an open question.

In this work we report anomalies observed on output characteristics of InAlAs / InGaAs HEMTs on InP substrate (degradation in drain current, Kink effect, Hysteresis effect, etc.). Defects analysis performed by Current and capacitance Deep Level Transient Spectroscopy (I - DLTS and C - DLTS); prove the presence of deep defects. These defects are strongly correlated to Kink and Hysteresis anomalies. So, the aim of this study is to confirm the relationship between Kink effect and InAlAs/InGaAs/InP HEMT's structure. We propose to clarify the main factor that causes the Kink. This allowed us to develop a physical new model which affirms the relation between Kink and defects in InAlAs/InGaAs/InP HEMT's.

2. Sample Details

The first sample ''S'' used in this work was grown by metal organic chemical vapor deposition (MOCVD). It is composed of a 1500 nm thick Si doped InxAl1-xAs layer grown by MOCVD on a doped InP substrate. The InxAl1-xAs material was grown with an alloy composition x = 0.52 to insure a good lattice matching to InP. This heterostructure was grown at a temperature of 700 °C. 500 µm diameter of Ti - Au is evaporated on the InAlAs top layer to make the Schottky contact. C-V measurements were carried out, at room temperature. The experimental built-in potential Vbi is found to be about 0.45 V. The doping concentration ND obtained from the same measurements is found to be equal to 5.9 ×1016 cm-3, which is in good agreement with [15].

The same structure has been developed to obtain different transistors. Two kinds of HEMT transistor have been analyzed in this work.

Fig. 1(a) shows the structure of the first HEMT transistor labelled ''S1'' which is mainly characterized in this paper. This transistor has a composite channel consisting of a 10 nm-thick InGaAs layer grown on the top of a 2 nm - thick InP spacer and a 20 nm - thick InP sub -channel. This structure can therefore combine the high mobility of InGaAsat low electric fields with the low impact ionization coefficient and the high electric drift velocity of InP at high electric fields [16, 17, and 18]. Lattice – matched InAlAs barrier and InGaAs cap layers have been finally grown on the top of this double channel structure.

Fig. 1(b) shows the structure of the second transistor, labelled ''S2''. In this structure, the undoped InP sub - channel is a 25 nm-thick containing δ-doping at 7 nm from the InGaAs channel.

These HEMT's with 0.8µm gate length were made using conventional lithography and a selective chemical etching for gate recess. The gate current is very low because of the non-doped InAlAs barrier. This result is required for base band photodetection applications and encourages the use of MOCVD technology in OEIC's design.

3. Results and Discussions

3.1. DLTS and Photoluminescence Measurements

DLTS measurements are performed in the temperature range 10-320 K using a He closed-cycle cryostat system. Measurements performed on sample "S" [24], show the presence of four traps A, B, C and D situated at 0.61 eV, 0.38 eV, 0.1 eV and 0.03 eV, respectively. Traps C and D are observed by PL technique.

DLTS measurements performed on sample ''S2'' [26], show the presence of two main traps A and B with activation energies closed to 0.75 eV and 0.34 eV, respectively. These are the same defects seen on sample S.

Fig. 2 shows a typical PL spectrum obtained for "S" sample measured at 10 K and for an incident power of 100 mW. This PL spectrum shows the presence of four main transitions. The transition at 1.51 eV is related to the InAlAs bulk material and is probably associated to band - band transition. Another transition at about 1.41 eV, which is not well clearly, is probably associated to the InP gap. This PL transition is not clearly shown in our case due to the broadening of the InAlAs PL peak[19], which is induced by the presence of the clusters in InAlAs material [20]. Two other transitions were observed, the first one is at 1.47 eV and the second is at 1.31 eV.

Defect A with an activation energy of 0.61 eV for sample "S" and 0.75 eV for sample "S2" respectively, can be attributed to defect E1 founded by Luo et al. [21] and Souifi et al. [15]. Oxygen may be the physical origin of defect A as shown by Naritsuka et al. [22]. This result was even confirmed by other authors [23, 24 and 25]. Furthermore, the concentration profile of this defect was determined by varying the bias voltage V0 and measuring the DLTS peak height. Fig. 3 shows that for a 0.22 µm in depth, the concentration remains constant. We conclude that defect A is not an interfacial defect but it is distributed uniformly in the bulk of the structure. The concentration of defect A is also measured by varying the filling pulse duration t p (Fig. 4). It is shown that it is approximately constant from t P = 1ms. We conclude that defect A is also a punctual defect.

Defect B appear on samples "S" and "S2" with activation energies close to 0.38 eV and 0.34 eV, respectively. These defects have been observed by Souifi et al. [15] and called E2. The concentration N T as a function of V 0 (Fig. 3) and N T as a function of t P, were realized on defect B and have shown the same behavior as defect A. SIMS measurements performed in CNET Bagneux [15]; confirm the strong correlation between defect B and

oxygen impurities concentration. Refeering to Luo et al. [25], defect B can be considered as an intrinsic defect.

The defect C appears with an activation energy equal to 0.1 eV. This defect may be identified as trap E3 found by different authors [15, 21]. A further investigation of this defect is realized by PL technique. PL Intensity is recorded as a function of temperature (Fig. 5). Four transitions are observed: 1.31 eV, 1.41 eV, 1.47 eV and ~ 1.51 eV. From the trace of the PL intensity as a function of 1 / T (Fig. 6) for the transition 1.47 eV, we deduce the activation energy for the corresponding defect from the relationship:

$$I_{PL} = \frac{I_0}{1 + A \exp(E_a / K T)} \quad (1)$$

Results give an activation energy value equal to 0.1 eV which is in a good agreement with value determined by DLTS technique. The activation energy of the capture cross-section has been measured and found to be EB = 25 meV (Fig. 7(a)), it can be considered as the DLTS measurement errors. We conclude that defect C observed by DLTS is related to transition 1.47eV observed by photoluminescence.

Defect D, appears with activation energy closed to 0.03 eV, observed in the first time by DLTS technique. It is observed for the sample "S" with high concentration. The capture cross-section of this defect does not seem to be thermally activated (Fig. 7(b)). The concentration profile of defect D is approximately uniform at a depth of about 0.22 µm (Fig. 3). Like defect A and B, trap D is uniformally distributed in InAlAs material. It is also shown that defect D is saturated after a filling pulse duration of 1 ms (Fig. 4); D is then a punctual defect. PL measurements are also realized in order to determine the physical origin of defect D. Fig. 6 shows the variation of the PL intensity of 1.31 eV transition, as a function of 1 / T. The resulting activation energy is 30 meV which is the same as that determined by DLTS. We conclude that defect D is associated to 1.31 eV transition.

In fact, detailed study of these defects by photoluminescence (PL) technique has led to the same results as those determined by DLTS which is confirmed by a previous work [26].

3.2. Current Deep Level Transient Spectroscopy (I-DLTS)

The gate surface of the studied transistors is very small (0.8µm×0.5µm) and (1µm×0.5µm), hence the gate capacitance is low. Therefore, it is not appropriate to use the Capacitance Transient Spectroscopy (DLTS) for deep levels analysis. Drain Current Transient Spectroscopy (I-DLTS) is a more reliable tool for our purpose. Since HEMT's are majority electron carrier devices, only electron traps can be detected in our case. The transistors are biased in the linear region. A reverse bias was applied on the gate and positive pulses were superimposed to probe the channel region and / or the barrier layer. Measurements were performed in 77- 400 K temperature range.

I-DLTS spectra are shown in [26] for "S1" sample. Two main traps called "A" and "B" are detected. Their activation energies extracted from Arrhenius diagrams are closed to 0.62 eV and 0.38 eV, respectively defect A and B. These are the same activation energies of defects, observed in "S" and "S2" samples.

Table 1 presents results concerning activation energies and cross-section values of the different traps, observed on samples ("S", "S1" and "S2").

3.3. Current-Voltage Static Measurements

Drain-source current-voltage I_{ds} - V_{ds} measurements as a function of gate voltage and temperature have been performed. For high temperature measurements we used a 600 K cryostat with liquid nitrogen circulation. The characteristics measured at different temperatures show several parasitic effects such as (leakage current, degradation in saturation current, Hysteresis effect, distortions for drain current in saturation region after high voltage applications…). These parasitic effects appear on output characteristics and they limits the good performance expected on InAlAs/InGaAs/InP HEMTs transistors. The pinced off voltage "V_t" extracted from I_{ds}-V_{gs} characteristics ranges from -0.5 to -0.8 V. It depends on the gate length and temperature.

The first anomaly observed on I_{ds} - V_{ds} characteristics is called "Kink effect", it consists of a sharp increase in the drain – source current at a particular drain – source voltage (V_{ds} =V_{Kink}). This increase in drain – source current induces an increase in the drain – source output conductance (G_{ds}). We have observed a spectacular Kink effect on transistor "S_2" with composite channel. This effect is observed at low temperatures and starts to appear from 100 K (Fig. 8). Increasing temperature, Kink effect disappears and I_{ds} - V_{ds} characteristics show standard variation standard without anomalies (Fig. 8). It is clear visible a reduction of I_{ds} and an enhancement of the Kink effect when the temperature decreases down to 100 K (Fig. 8).

I_{ds}- V_{ds} characteristics of the InGaAs/InP double channel HEMT "S_1" are determined at different temperatures and for different gate - source voltages "V_{gs}". The results are shown in Fig.9. We can easily notice the presence of a double Kink effect in the I_{ds} - V_{ds} characteristics, especially at low temperatures Fig. 9; whereas at high temperatures this effect disappears. If we plot the variation of the Kink current ΔI_{d02} as a function of temperature (Fig. 10) we notice the presence of peak at about 250 K. We can then attribute the second parasite effect observed in I_{ds} - V_{ds} characteristics to defect "A" which appears at the same range of temperature. Whereas, defect "B" is observed in the range of temperature varying from 170 K to 210 K. The variation of the Kink current ΔI_{d01}, of the first Kink effect observed in I_{ds} - V_{ds}, as a function of temperature (Fig. 10) shows the presence of one peak at a temperature of about 200K. We can then confirm the correlation between defect "B" observed by C-DLTS technique with the first parasitic

Kink effect observed in I_{ds} (V_{ds}) characteristics, in our previous work [27].

The second parasitic effect observed in this study is Hysteresis effect; it is characterized by a shift of the I_{ds} - V_{ds} curve when the gate voltage varies in one way and then back. This shift is well observed at low temperature (Fig. 11), whereas it is absent at high temperature. The area separating the two go-return I_{ds} - V_{ds} curves, plotted as a function of temperature (Fig. 12) shows the presence of one peak at a temperature in the order of about 200 K. we can then attribute the Kink and the Hysteresis effects to the presence of defect B in "S_1" sample.

The third parasitic effect observed on InAlAs/InGaAs/InP HEMTs consists in a distortion on I_{ds} - V_{ds} characteristics in the saturation region after a stress application (the stress consists in an application of 3V between drain and source contacts for 5 min). Fig. 13 shows I_{ds} - V_{ds} characteristics measured on InAlAs/InGaAs/InP HEMT after a stress application. These effects become important for high temperatures (400 K). If we let transistors in rest and we take again I_{ds}- V_{ds} measurements, distortion on the drain current in the saturation region will disappear. These measurements are reproductible. A possible hypothesis about the origin of this effect is traps. Traps are thermally activated and their charge state changes when we change temperature. These traps charge and discharge carriers and act on output characteristics. From physics point of view, these traps are represented by a variable resistance. In terms of charge, applying stress consists in a modification of the global charge of traps. I_{ds} - V_{ds} characteristics reveal a spectacular deformation in drain current after a stress application (V_{ds} = 3V for 5 min). Traps are uniformly charged after a stress application and the distribution of traps can be assimilated to a fictive resistance that gives the distortion on I_{ds} - V_{ds} characteristics. We confirm, in our previous work [28], that the value of this fictive resistance depends on the charge state of the traps.

3.4. Physical Model for the Kink Effect

Kink effect is a problem not only in InAlAs/InGaAs HEMTs, but also in AlGaAs/GaAs, AlGaAs/InGaAs HEMTs and HFETs [29, 30] and silicon – on insulator metal – oxide – semiconductor FETs (SOI- MOSFETs). In these structures a general explanation for Kink effects has not been formulated yet, possibly due to the fact that the Kink can be due to different mechanisms. Moreover, the Kink is remarkably dependent on growth and process conditions, and sometimes has different characteristics in devices even on the same wafer [31, 32, and 33]. Kink is a frequency – dependent phenomenon, which is sometimes correlated with dependence of transconductance on frequency at low frequency (transconductance dispersion, gm(f)), with transients in drain current when the drain or gate voltage is pulsed (drain- or gate- lag, respectively), with frequency dispersion of output conductance (gD(f)) [13, 14]. Most recent models of Kink effect are based on the effect of holes, generated by impact ionization and accumulated at the extrinsic source [34]. These models suggest that the Kink arises from process in which impact ionization generated holes travel from the drain - gate region through the intrinsic device and pile up in the extrinsic source. This hole leads to a whole current to the surface and / or the buffer – substrate interface, which in turn changes the charge in these locations. As a result, the channel potential and electron concentration are raised, resulting in a shift in threshold voltage and extra gate drive to the transistor.

Several studies of the Kink phenomenon have been recently carried out, including dc characterization, side-gate measurements [31], and large-signal transient measurements with nanosecond resolution [35]. It is of interest to drive a model for Kink effect, because this parasitic effect often appears. This has allowed us to develop a dynamic physical model, by MALTLAB language, for the Kink effect in InAlAs/InGaAs HEMT transistor growing by MOCVD on a doped InP substrate.

By neglecting diffusion contributions, the drain current Ids are giving by the usual equation:

$$I_{ds} = Z e n \upsilon \tag{2}$$

Where, "Z" is the gate width, "e" the electronic charge magnitude, "υ" the electron velocity in the channel, which is assumed to be a function of the electronic field "E" in the channel, expressed by this equation: $\upsilon = -\mu E = \mu \frac{dV}{dy}$, where y is the canal width, μ is the mobility of electron, E is the electric field, V is a voltage, and n represents the density of electrons, which is given by the following equation [36]:

$$n = \beta (V_{gs} - V_t - V) \tag{3}$$

Vgs represents the gate - source voltage, "V" is a voltage depending on y which vary from V=0, by side source, to V = Vd, by side drain, and Vt is the threshold of voltage.

Where

$$\beta = \frac{2 \varepsilon e m_e}{2 d e^2 m_e + \varepsilon \pi \hbar^2} \tag{4}$$

ε is the permittivity, me is the electron mass, d is the thickness of the transistor until the canal, e is the electron charge and ħ is the Planck constant.

The drain – source current Ids as function of the drain – source voltage Vds, in the linear region ($V_{ds} < V_{dsat}$) can be evaluated by combining (1) and (2) equations. Then, we obtain:

$$I_{ds} = \frac{Z e \beta \mu}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \tag{5}$$

In order to calculate the characteristics in the saturation region, the channel length modulation effect must be taken into account. When the 2 - DEG carriers are accelerated to

the saturation velocity by the longitudinal electrical field parallel to the current flow, the 2-DEG channel current in the saturation region is expressed by the equation [37]:

$$I_{dsat} = g_0 \left[\left(\sqrt{V_s^2 + (V_{gs} - V_t)^2} - V_s \right) \right] \quad (6)$$

Where

$$g_0 = Z e \beta \mu E_s \quad (7)$$

And E_s is the critical electrical field at y = L.

By increasing V_{ds}, hot electrons of the two dimensional electron gas (2-DEG) gain enough kinetic energy from the accelerating electric field in the channel to surmount the InAlAs/InGaAs energy barrier [38, 39] and get then captured by donor related deep traps (N_T^+). As V_{ds} is increased enough, approximately to V_{kink}, the carriers trapped in the high field gate to drain region are realised. This electric field should be high enough to cause the traps filled with electrons and an increase of the dissipated power, so that the detrapping mechanisms are thermally activated [40, 41, 42 and 43]. The decrease of negative charge lowers the potential barrier, which controls the number of carrier crossing the channel, and consequently leads to a sudden rise in Ids.

This phenomenon causes a change of the expression of the density of electron in 2-D electron gas (2). The new electron density when taking account the concentration of ionized traps (N_T^+) is giving by this equation:

$$n' = N_T^+ + \beta (V_{gs} - V_t - V_d) \quad (8)$$

This can be written:

$$n' = \beta' (V_{gs} - V_t - V_d) \quad (9)$$

Where

$$\beta' = \beta + \frac{N_T^+}{V_{gs} - V_t - V_d} \quad (10)$$

When, we replace β' by its expression (9), we can obtain the expression for the drain current in the saturation region when $V_{dsat} \geq V_{kink}$. For a certain tension $V_{ds} = V_{kink}$, the electron traps participate to the conduction phenomena. Taking account of this hypothesis and the same stages of calculate of I_{dsat}, we can then, determined the drain – source current in the saturation region, when $V_{dsat} \geq V_{kink}$:

$$I_{dsat}' = g_0 \left[\left(\sqrt{V_S^2 + \left(\frac{N_T^+}{\beta} + V_g - V_t \right)^2} - V_S \right) \right] \quad (11)$$

As V_{ds} becomes equal to V_{kink}, field assisted carrier detrapping phenomena at the drain side of the gate causes the Kink effect. For this reason, we must determine the expression of the N_T^+ concentration.

The principle of the detailed energy balance equations is giving by:

$$n g_T W_{E_C \to E_T} N_T^+ = (N_C - n) W_{E_T \to E_C} N_T^\circ \quad (12)$$

Where n is the electron density, g_T is a factor of degeneration which is equal to 2, EC represent the conduction band edge energy, which is taken the 0 value as a reference of energies, and ET is the energy of the trap level. $W_{E_C \to E_T}$ *and* $W_{E_T \to E_C}$ Represent the energy density loss rates for electrons and holes, respectively. N_T^+ *and* N_T° Are donor ionized and non ionized concentration traps.

By applying certain assumptions, the Boltzmann statistics and the hypothesis that the material is non degenerate, the concentration of ionized trap level can be evaluated by the following equation:

$$N_T^+ = \frac{N_T}{1 + g_T \exp\left(\frac{E_F - E_T}{K T} \right)} \quad (13)$$

From charge neutrality in a system containing N_D^+ shallow donor, N_A^- shallow acceptor, and N_T^+ deep donor, we can write:

$$n + N_A^- = p + N_D^+ + N_T^+ \quad (14)$$

In our case, the material is n type then p is neglected by report n. The shallow donors are mostly ionized and acceptors are neglected. Thus $N_D^+ \approx N_D$ and $N_A^- \approx 0$.

In this case, the equation of neutrality becomes:

$$n = N_D - N_T^+ \quad (15)$$

If we combining equations (12) and (14), we can obtain an equation of the 2nd degree. The resolution of this equation gives the ionized trap level concentration as a function of the temperature:

$$N_T^+ = -\frac{1}{2}\left(N_D + \frac{N_C}{2} e^{(E_T/KT)} \right) + \frac{1}{2}\sqrt{\left(\frac{N_C}{2} e^{(E_T/KT)} - N_D \right)^2 + 2 N_C N_T e^{(E_T/KT)}} \quad (16)$$

Figure 14 shows the evolution of the ionized trap concentration as a function of temperature. We can, then, inject the expression (15) of the concentration N_T^+ in equation (10) of the drain–source current to obtain Ids - Vds characteristics according to temperature.

In this section, we present a comparison between simulated I_{ds} - V_{ds} characteristics using the model described above and experimental data of structure "S2", which contains one Kink effect. Taking account of the activation energy of trap "B" and the Kink voltage (V_{Kink}), determined experimentally, we have plotted simulated I'_{dsat} - V_{ds} for different temperatures (Fig. 15). We can see an

excellent agreement between the simulation results and experimental measurements of the I_{ds} - V_{ds} characteristics obtained for low temperature and high temperature. These results are in a good agreement with the hypothesis which confirms the influence of deep levels, present in InAlAs/InGaAs/InP HEMT transistor, on the Kink and Hysteresis effects observed in all I_{ds} -V_{ds} characteristics.

4. Conclusion

In summary, deep levels in InAlAs/InGaAs/InP heterojunction HEMTs were directly studied by means of capacitance and current DLTS techniques. Mainly two defects called "A" and "B" with activation energies of 0.62 ± 0.05 eV and 0.38 ± 0.04 eV respectively, were observed in all samples. DLTS measurement shows also the presence of two other defects, C and D, observed only in InAlAs material with activation energies equal to 0.1 eV and 0.03 eV, respectively.

I_{ds} - V_{ds} measurements were also performed on the same transistors; they have shown the presence of Kink and Hysteresis effects in the structure. The study of "S1" HEMT has shown the presence of a double Kink effect. The first Kink effect has been correlated to the defect "B" detected at 0.38 eV, while the second Kink effect is correlated to defect "A" detected at 0.62 eV.

We have developed a new theoretical approach allowing us to simulate the drain - source current as a function of temperature. This approach takes account the contribution on the channel conduction of carrier thermal emission from the traps. A good agreement between the simulation results and the experimental measurements of the I_{ds} - V_{ds} characteristics is obtained. We can then confirm that trapping and detrapping mechanisms are the physical origin of the apparition of the Kink and Hysteresis effects observed on the output HEMT characteristics.

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